REMARKS/ARGUMENTS

Claims 1, 2, 4, 6 and 8 are currently pending in this application.

Claim Rejections - 35 USC §103

Claims 1-2, 4, 6, and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,115,410 to Naruse (hereinafter "Naruse"), in view of U.S. Patent No. 6,798,737 to Dabak et al. (hereinafter "Dabak").

Naruse relates to a Walsh code generator, including a binary counter, a parallel generation controller, and a Walsh code parallel generator. The counter controls the position of an output bit in the Walsh code. The parallel generation controller controls an upper portion of the Walsh code, and the Walsh code parallel generator controls a lower portion of the Walsh code. The parallel generator controller includes a plurality of AND gates, the outputs of the AND gates being connected to a plurality of XOR gates. (See Figures 3-4 and column 5, lines 26-67.)

Dabak relates to a method of performing a Walsh-Hadamard transform for forward link multiuser detection in CDMA. Specifically, Dabak teaches using inverse Walsh code transformations to separate channels containing Walsh coding for a plurality of channels. Dabak does not teach the actual generation of the Walsh codes.

Pending claims 1, 4, 6, and 8 teach the generation of Orthogonal Variable Spreading Factor (OVSF) codes include the element of inputting the bits in order from most significant bit to least significant bit, and reordering the bits from least significant bit to most significant bit. The Examiner has cited Dabak, column 4, lines 52-66 as teaching this element; however, the Applicant respectfully disagrees. The cited section of the reference states:

> The IMFWT requires only the number of operations (or fewer) corresponding to the largest spreading factor. Thus, if spreading factors of 32 and 128 are present as in the earlier example, then the number of operations required to process 256 chips is 1792 or less. There can be fewer operations since some of the butterflies are not required in the multi-rate FWTs. For the Walsh codes with lower spreading factors, the inputs which use the same Walsh code must be in bit-reversed order of the indices as demonstrated by x4, x5, x6 and x7 in FIG. 3. (Dabak column 4, lines 53-62, emphasis added).

The cited section refers to the "inputs which use the same Walsh code" being in bit-reversed order, not the Walsh code itself being in bit-reversed order. Clearly this is not the same as inputting the bits in order from most significant bit to least significant bit, and reordering the bits from least significant bit to most significant bit.

Further, Dabak relates to efficiently performing a fast Walsh transform (FWT) and inverse multi-rate fast Walsh transform (IMFWT, see column 3, lines 18-25). In order to perform a FWT or IMFWT, the applicable Walsh code must already be determined. The present invention is related to generating OVSF codes

which may then be used in a transform similar to the FWT. Dabak does not teach or suggest any of the elements of the present invention simply because it relates to performing operations on Walsh codes, and not generating the codes themselves. Therefore, the combination of Naruse and Dabak does not teach or suggest all of the elements of claims 1, 4, 6, and 8.

Pending claim 2 contains the reverse step, inputting the bits in order from least significant bit to most significant bit, and reordering the bits from most significant bit to least significant bit. As explained above, neither Naruse nor Dabak teach reordering the bits in this manner.

Based on the arguments presented above, withdrawal of the §103(a) rejection of claims 1, 2, 4, 6, and 8 is respectfully requested.

Conclusion

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing remarks, Applicant respectfully submits that the present application, including claims 1, 2, 4, 6, and 8, is in condition for allowance and a notice to that effect is respectfully requested.

Respectfully submitted,

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